Performance evaluation of Graph500 considering CPU-DRAM power shifting

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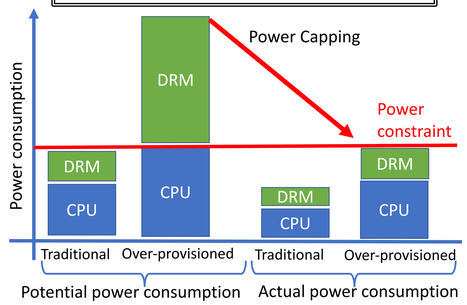
1. Introduction and Motivation

Computing demands on a power constraints

Ex1) Over Provisioned System



- Over-provisioned system has too much hardware than its capacity of the power source.
- The actual power consumption of the components must be controlled by a power capping technique in order not to violate the power constraint.

Ex2) Social Demands

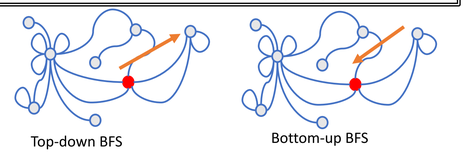
There are some social demands for power constraints.

For example,
- Ability of an electricity generating station.
- Power contract of building.

We need to shift power appropriately for each hardware component

Emerging Application (Graph500)

Direction-optimized BFS (Hybrid of Top-down and Bottom-up approach)

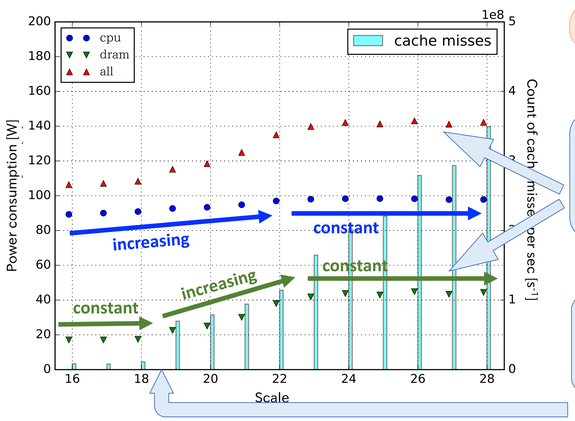


- A graph analysis is increasing its importance with growing big data applications.
- A large scale graph processing app. is executed on an overprovisioning system.
- It is not revealed the performance impact of graph applications under power constraints.

Need to know the impact of power capping on Graph500 performance!

2. Basic Power Analysis

Impact of input sizes on CPU/DRAM power

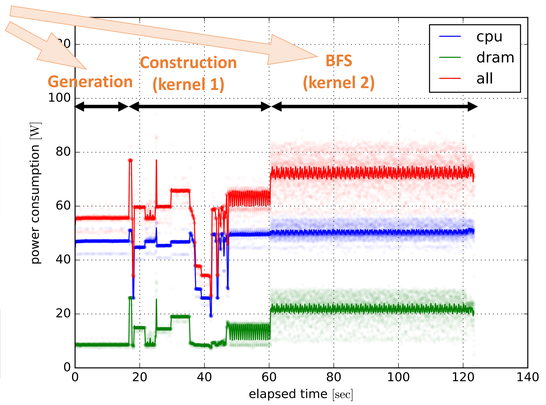


These kernels forms a phase each.

The power consumption of DRAM strongly affects dependency of overall power consumption on problem size than the power consumption of CPU.

The power consumption of DRAM is increasing with the increase of the count of access to DRAM.

Dynamic behavior of power consumption



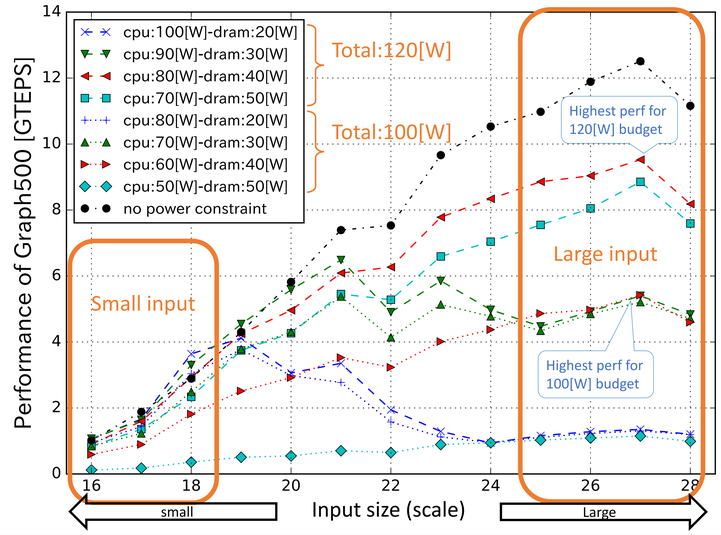
Experimental environment

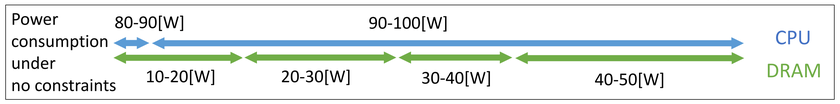
CPU	Intel Xeon E5-2620 (6core) x2, TDP 95[W]
Memory	16GB x8 (128GB)
Compiler	Intel Compiler Version 14.0.0
Power MGMT	RAPL

Power consumption of BFS kernel forms a phase. Do not need to concern about changing the amount of power shifting during execution of BFS.

3. Impact of CPU/DRAM Power Capping

Performance of Graph500 under power constraint





Relatively small input
- Preferentially shifting power to CPU brings higher performance.
- The power consumption of DRAM is less than the fewest power budget for DRAM in this range, so power shifting to DRAM is enough.
  - The power constraints of DRAM are more than or equal to 20[W].
  - The power consumption of DRAM is also less than 20[W] under no power constraint setting.

Relatively large input
- Preferentially shifting power to DRAM brings higher performance.
- The power consumption of DRAM is up to 40[W].
- Allotting 40[W] to DRAM brings highest performance for 25 <= scale <= 27.
- However, allotting 50[W] to DRAM and 50[W] to CPU brings worst performance.

Good power shifting depends on input size

4. Summary

- The power consumption of DRAM is increasing in specific range.
- Good power budgeting depends on input size.
- Importance of shifting power budget to DRAM is increasing with the increase of input size.